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25. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having a first surface voltage;

a second layer of material formed on the first layer, the second layer having a second surface voltage, the second surface voltage being different than the first surface voltage; and

a metallization layer formed on the second layer.

26. (New) The integrated circuit of claim 25, wherein the metallization layer comprises non-alloy copper.

27. (New) The integrated circuit of claim 25, wherein the first layer comprises poly-silicon and the second layer comprises titanium nitride.

28. (New) The integrated circuit of claim 25, wherein the first surface voltage is lower than the second surface voltage.

29. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate;

an insulator layer formed on the first layer, the insulator layer and the first layer having contact vias;

a second layer formed on the first layer, the second layer lining the contact vias; and

a metallization layer on the second layer.

30. (New) The integrated circuit of claim 29, wherein the metallization layer on the second layer fills the contact vias.

31. (New) The integrated circuit of claim 29, wherein the first layer and the second layer have exposed surfaces upon which voltage may be applied.

32. (New) A semiconductor manufacturing system, comprising:

means for forming a first layer overlying a substrate;

means for forming contact vias through the first layer to the substrate;

means for forming a second layer overlying the first layer and lining the contact vias; and

means for forming a metallization layer.

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33. (New) The semiconductor manufacturing system of claim 32, wherein the means for forming a metallization layer includes means for filling the contact vias.

34. (New) The semiconductor manufacturing system of claim 32, wherein the means for forming a metallization layer includes means for applying a bi-polar modulated voltage between the substrate and an anode in the presence of a electrolytic bath.

35. (New) A semiconductor manufacturing system, comprising:

means for providing a semiconductor device having:

a substrate;

a first layer overlying the substrate; and

a second layer overlying the first layer, wherein the device has an exposed first layer portion and an exposed second layer portion;

means for providing a bi-polar modulated voltage between the substrate and an anode in the presence of an electrolytic bath containing metal ions, wherein the modulated voltage has a positive duty cycle and a negative duty cycle;

wherein the metal ions are deposited on the exposed first layer portion and the exposed second layer portion during the positive duty cycle; and

wherein the metal ions are removed from the exposed first layer portion during the negative duty cycle.

36. (New) The semiconductor manufacturing system of claim 35, wherein the first layer comprises poly-silicon and the second layer comprises titanium nitride.

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37. (New) A semiconductor manufacturing system, comprising:

an electrolytic bath containing metal ions;

an anode;

a voltage supply, wherein the voltage supply provides a bi-polar modulated voltage between a substrate of a semiconductor device and the anode in the presence of the electrolytic bath, and wherein the modulated voltage has a positive duty cycle and a negative duty cycle;

wherein the metal ions are deposited on an exposed first layer of the semiconductor device and on an exposed second layer of the semiconductor device during the positive duty cycle; and

wherein the metal ions are removed from the exposed first layer during the negative duty cycle.

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38. (New) The semiconductor manufacturing system of claim 37, wherein the first layer has a first surface voltage and the second layer has a second surface voltage, and wherein the first surface voltage is lower than the second surface voltage.

39. (New) A method of forming an integrated circuit, comprising:

providing a semiconductor substrate;

forming a first layer overlying the substrate;

forming a second layer overlying the first layer to form an exposed first layer and an exposed second layer;

depositing metal ions on the exposed first layer and on the exposed second layer by applying a first voltage between the substrate and an anode in the presence of an electrolytic bath; and

removing metal ions from the exposed first layer by applying a second voltage between the substrate and the anode in the presence of the electrolytic bath.

40. (New) The method of claim 39, wherein forming the first layer overlying the substrate includes forming contact vias that extend through the first layer to the substrate.

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41. (New) The method of claim 39, wherein the method is performed in the order presented.

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42. (New) A method of forming an integrated circuit, comprising:

providing a semiconductor device having:

a substrate;

a first layer overlying the substrate;

a second layer overlying the first layer, wherein the device has an exposed first layer and an exposed second layer; and

providing a bi-polar modulated voltage between the substrate and an anode in the presence of an electrolytic bath containing metal ions,

wherein the modulated voltage has a positive duty cycle and a negative duty cycle;

wherein the metal ions are deposited on the exposed first layer and the exposed second layer during the positive duty cycle; and

wherein the metal ions are removed from the exposed first layer during the negative duty cycle.

43. (New) The method of claim 42, wherein the first layer comprises poly-silicon and the second layer comprises titanium nitride.

44. (New) The method of claim 42, wherein the method is performed in the order presented.

45. (New) A method of forming an integrated circuit, comprising:

providing a semiconductor substrate;

forming a first layer overlying the substrate;

forming an insulating layer overlying the first layer;

forming a second layer overlying the insulating layer, wherein the first layer includes an exposed first layer and the second layer includes an exposed second layer;

depositing metal ions on the exposed first layer and on the exposed second layer by applying a first voltage between the substrate and an anode in the presence of an electrolytic

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bath; and

removing metal ions from the exposed first layer by applying a second voltage between the substrate and the anode in the presence of the electrolytic bath.

46. (New) The method of claim 45, wherein the method is performed in the order presented.

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47. (New) A method of forming an integrated circuit, comprising:

providing a substrate;

providing a first layer overlying the substrate, wherein the first layer has contact vias;

forming a second layer, wherein the second layer lines the contact vias;

forming a metallization layer overlying the second layer; and

filling the contact vias.

48. (New) A method of forming an integrated circuit, comprising:

providing a substrate;

providing a first layer overlying the substrate, wherein the first layer has contact vias;

forming a second layer, wherein the second layer lines the contact vias; and

performing a single electro-deposition step to form a metallization layer and fill the contact vias.

49. (New) A method for depositing copper on a semiconductor device having a substrate, an exposed first surface, and an exposed second surface, comprising:

depositing metal ions on the exposed first surface and on the exposed second layer by applying a first voltage between the substrate and an anode in the presence of an electrolytic bath; and

removing metal ions from the exposed first surface by applying a second voltage between the substrate and the anode in the presence of the electrolytic bath.

50. (New) The method of claim 49, further comprising applying a first surface voltage to the first exposed surface and a second surface voltage to the second exposed surface.

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51. (New) The method of claim 49, wherein the method is performed in the order presented.

52. (New) A method for depositing copper on a semiconductor device having a substrate, an exposed first surface, and an exposed second surface, comprising:

providing a voltage with a positive duty cycle between the substrate and an anode in the presence of an electrolytic bath containing metal ions to deposit the metal ions on the exposed first layer and the exposed second layer during the positive duty cycle; and

providing a voltage with a negative duty cycle between the substrate and an anode in the presence of the electrolytic bath to remove the metal ions from the exposed first layer during the negative duty cycle.

53. (New) The method of claim 52, further comprising applying a first surface voltage and a second surface voltage.

54. (New) The method of claim 52, wherein the first layer comprises poly-silicon and the second layer comprises titanium nitride.

The Examiner is invited to telephone the Applicant's attorney (612) 373-6960 to facilitate prosecution of this application.

Respectfully submitted,

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Name Tina Pugh Signature